CLAIM AMENDMENTS

1. (currently amended) A spread spectrum digital communication receiver, the receiver comprising: [[-]]

an input memory buffer [[(16)]] for storing samples of an input signal [[(y(k))]]; [[-]]

a code generator circuit [[(30)]] for generating a re-generated user code; [[-]]

a device [[(24)]] for the estimation of a channel delay profile energy, for computing the time delays and amplitudes of each received multi-path component of said input signal [[(Y(k))]]; [[-]]

a plurality of fingers [[(18)]]; [[-]] and

a finger allocation unit [[(26)]] for processing said channel delay profile energy in order to select the strongest multi-path components of said input signal [[(y(k))]] and allocate them to said fingers [[(18)]]; ~~characterized in that said~~ wherein the device [[(24)]] for the estimation of a channel delay profile energy comprises: [[-]]

a basic correlator [[(32)]] having a first input [[(41)]] for sequentially reading from a memory location of said input memory buffer [[(16)]] a plurality of samples of said input signal [[(y(k))]], a second input [[(43)]] for receiving from said code generator circuit [[(30)]] a regenerated user code, and an output terminal for generating, by means of a correlation operation

between said plurality of samples of said input signal and said regenerated user code, a value of said channel delay profile energy [[(DP(1))]]; [[-]] and

a memory controller circuit [[(36)]] for addressing said input memory buffer [[(16)]] so that said first input [[(41)]] of said basic correlator [[(32)]] is successively fed with the content of the memory locations of said memory buffer [[(16)]], each addressing operation corresponding to a new correlation operation of said basic correlator [[(32)]] for the computation of a new value of said channel delay profile energy [[(DP(1))]].

2. (currently amended) The [[A]] receiver according to claim 1, wherein the values of said channel delay profile energy [[(DP(1))]] are progressively stored in a profile accumulation memory [[(34)]].

3. (currently amended) The [[A]] receiver according to claim 2, wherein said memory controller circuit [[(36)]] addresses said profile accumulation memory [[(34)]] so that the reading operations of said basic correlator [[(32)]] from said input memory buffer [[(16)]] and the writing operations into said profile accumulation memory [[(34)]] are handled by the memory controller circuit [[(36)]].

4. (currently amended) The [[A]] receiver according to claim 3, wherein said memory controller circuit [[(36)]] updates the addressing of said input memory buffer [[(16)]] and said profile accumulation memory [[(34)]] every NC chips, where NC is equal to the integration window size, changing the reading and writing positions of said basic correlator [[(32)]].

5. (currently amended) The [[A]] receiver according to claim 3, wherein, when the last memory location of both said input memory buffer [[(16)]] and said profile accumulation memory [[(34)]] is reached, the addressing restarts circularly on a first location of both memories [[(16, 34)]].

6. (currently amended) The [[A]] receiver according to claim 3, wherein said basic correlator [[(32)]] is time multiplexed, at a multiple of the chip frequency [[(F_c)]], between a plurality of memory locations of said input memory buffer [[(16)]] and of said profile accumulation memory [[(34)]].

7. (currently amended) The [[A]] receiver according to claim 2, wherein said delay profile energy [[($DP_{acc}(1)$)]] is obtained by accumulating the energies [[($DP_i(1)$)]] of several delay profiles.

8. (currently amended) A method for the estimation of the channel delay profile energy in a spread spectrum digital communication receiver of the type comprising an input memory buffer [[(16)]] for storing samples of an input signal [[(y(k))]] and a code generator circuit [[(30)]] for generating a re-generated user code, the method comprising the steps of:

a) sequentially reading a first plurality of samples of the input signal y(k) from said memory buffer 16;

b) correlating said plurality of samples of said input signal with said regenerated user code for generating a first value of the channel delay profile energy [[(DP(k))]];

c) updating the reading position on said input memory buffer [[(16)]] for reading a further plurality of samples of the input signal [[(y(k))]];

d) correlating said further plurality of samples of said input signal with said regenerated user code for generating a further value of the channel delay profile energy [[(DP(k+1))]], said generated value of the channel delay profile energy [[(DP(k+1))]] being stored in a profile accumulation memory [[(34)]]; and

e) repeating the steps c)]] to d)]] in order to compute all the values of the channel delay profile.

9. (currently amended) The [[A]] method according to claim 8, further comprising the step of

storing each generated value of said channel delay profile energy [[(DP(1))]] in a profile accumulation memory [[(34)]].

10. (currently amended) A spread spectrum digital communication receiver, the receiver comprising: [[-]]

a code generator circuit [[(52)]] for generating a re-generated user code; [[-]]

a memory buffer [[(50)]] for storing samples of said re-generated user code; [[-]]

a device [[(64)]] for the estimation of a channel delay profile energy, for computing the time delays and amplitudes of each received multi-path component of an input signal [[(y(k))]] received by said receiver; [[-]]

a plurality of fingers [[(78)]]; [[-]] and

a finger allocation unit [[(76)]] for processing said channel delay profile energy in order to select the strongest multi-path components of said input signal [[(y(k))]] and allocate them to said fingers [[(78)]]; ~~characterized in that said~~ wherein the device [[(64)]] for the estimation of a channel delay profile energy comprises: [[-]]

a basic correlator [[(54)]] having a first input [[(41)]] for receiving said input signal [[(y(k))]] and a second input

[[(43)]] for sequentially reading from a memory location of said memory buffer [[(50)]] a plurality of samples of said re-generated user code, and an output terminal for generating, by means of a correlation operation between said input signal and said plurality of samples of said regenerated user code, a value of said channel delay profile energy [[(DP(1))]]; [[-]] and

a memory controller circuit [[(58)]] for addressing said memory buffer [[(50)]] so that said second input [[(43)]] of said basic correlator [[(54)]] is successively fed with the content of the memory locations of said memory buffer [[(50)]], each addressing operation corresponding to a new correlation operation of said basic correlator [[(58)]] for the computation of a new value of said channel delay profile energy [[(DP(1))]].

11. (currently amended) The [[A]] receiver according to claim 10, wherein the values of said channel delay profile energy [[(DP(1))]] are progressively stored in a profile accumulation memory [[(56)]].

12. (currently amended) The [[A]] receiver according to claim 11, wherein said memory controller circuit [[(58)]] addresses said profile accumulation memory [[(56)]] so that the reading operations of said basic correlator [[(54)]] from said memory buffer [[(50)]] and the writing operations into said profile accumulation memory [[(56)]] are handled by the memory controller circuit [[(58)]].

13. (currently amended) The [[A]] receiver according to claim 12, wherein said memory controller circuit [[(58)]] updates the addressing of said memory buffer [[(50)]] and said profile accumulation memory [[(56)]] every NC chips, where NC is the integration window size, changing the reading and writing positions of said basic correlator [[(54)]].

14. (currently amended) The [[A]] receiver according to claim 12, wherein, when the last memory location of both said memory buffer [[(50)]] and said profile accumulation memory [[(56)]] is reached, the addressing restarts circularly on a first location of both memories [[(50, 56)]].

15. (currently amended) The [[A]] receiver according to claim 12, wherein said basic correlator [[(54)]] is time multiplexed, at a multiple of the chip frequency [[(F_c)]], between a plurality of memory locations of said memory buffer [[(50)]] and of said profile accumulation memory [[(56)]].

16. (currently amended) The [[A]] receiver according to claim 12, wherein said delay profile energy [[($DP_{acc}(1)$)]] is obtained by accumulating the energies [[($DP_i(1)$)]] of several delay profiles.

17. (currently amended) A method for the estimation of the channel delay profile energy in a spread spectrum digital communication receiver of the type comprising a code generator circuit [[(52)]] for generating a re-generated user code and a memory buffer [[(50)]] for storing samples of said re-generated user code, comprising the steps of:

a) sequentially reading a first plurality of samples of the re-generated user code from said memory buffer [[(50)]];

b) correlating said plurality of samples of said re-generated user code with an input signal y(k) for generating a first value of the channel delay profile energy [[(DP(k))]];

c) updating the reading position on said input memory buffer [[(50)]] for reading a further plurality of samples of the re-generated user code;

d) correlating said further plurality of samples of said re-generated user code with said input signal [[y(k)]] for generating a further value of the channel delay profile energy [[(DP(k+1))]], said generated value of the channel delay profile energy [[(DP(k+1))]] being stored in a profile accumulation memory [[(56)]]; and

e) repeating the steps c)]] to d)]] in order to compute all the values of the channel delay profile.

18. (currently amended) The [[A]] method according to claim 17, further comprising the step of storing each generated value of said channel delay profile energy [[(DP(1))]] in a profile accumulation memory [[(56)]].